CLAIMS

1. A packet switched communications system for transmitting synchronous data from a source module to a terminating module over a network comprising plurality of modules interconnected via transmission links, each module operating with a clock of nominal frequency but which is not synchronised with the clocks of the other module(s)and having a single input and one or more outputs where all the outputs are phase locked to each other but are not synchronised with respect to the input, means for determining the accumulated phase difference between the input clock and the output clock of each module, means for transmitting the accumulated phase difference to the terminating module in the network, and means for utilising the received accumulated phase difference at the terminating module to lock the output clock at the terminating module to the input clock at the source module.

2. A system as claimed in Claim 1 in which the accumulated phase difference is transmitted at regular intervals in an ATM data cell.

3. A system as claimed in Claim 1 or Claim 2 in which the determining means comprises a first counter for counting clock cycles of the input signal clock, a second counter for counting cycles of the output signal clock, and means for simultaneously reading the counts of the first and second counters.

4. A system as claimed in Claim 3 comprising a latch for storing the count of the counter counting the

higher frequency clock, the count being clocked into the latch by an edge of the lower frequency clock.

5. A system as claimed in any of Claims 3 or Claim 4 in which the means for transmitting the phase difference comprises means for assembling an ATM cell containing the counts of the first and second counters

6. A method of recovering clock signals in a packet switched communications network, the network comprising a plurality of modules interconnected via transmission links, each module operating with a clock of nominal frequency but which is not synchronised with the clocks of the other module(s)and having a single input and one or more outputs where all the outputs are phase locked to each other but are not synchronised with respect to the input, the method comprising the steps of:

a) determining the accumulated phase difference between the input clock and the output clock at each module,

b) transmitting the determined accumulated phase difference to the terminating module, and

c) utilising the received accumulated phase difference at the terminating network to recover the clock at the source module of the network.

7. A method as claimed in Claim 6 in which the network uses asynchronous transfer mode (ATM) and the accumulated phase difference is transmitted in an ATM cell

8. A method as claimed in Claim 6 or Claim 7 in which step a) comprises the steps of:

d) applying the input clock of a module to a first counter within the module,

e) applying the output clock of the module to a second counter within the module,

f) reading the counts of the first and second counters simultaneously at given intervals.

9. A method as claimed in Claim 8 in which step d) comprises transmitting the counts read in step f).

10. A method as claimed in Claim 8 or Claim 9 in which the counters are read on a transition of the lower frequency clock.